IN THE CLAIMS:

Claims 1-6, 8-25, 27-44, 46-54, 56-59, and 61-72 been amended. All of the pending claims 1 through 72 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Currently Amended) An integrated circuit device comprising:

a first conductive layer including at least one protrusion;

an insulative layer overlying ~~said~~ the first conductive layer and exposing at least part of ~~said~~ the at least one protrusion; and

a programmable resistive material in direct contact with ~~said~~ the at least one protrusion of ~~said~~ the first conductive layer.

2. (Currently Amended) The integrated circuit device of claim 1, wherein ~~said~~ the programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

3. (Currently Amended) The integrated circuit device of claim 1, wherein ~~said~~ the exposed part of ~~said~~ the at least one protrusion comprises a smaller cross-sectional area than a remaining part of ~~said~~ the at least one protrusion of ~~said~~ the ~~at least one~~ first conductive layer.

4. (Currently Amended) The integrated circuit device of claim 1, wherein ~~said~~ the programmable resistive material comprises a chalcogenide material.

5. (Currently Amended) The integrated circuit device of claim 4, wherein ~~said~~ the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

6. (Currently Amended) The integrated circuit device of claim 4, wherein ~~said~~ the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

7. (Original) The integrated circuit device of claim 6, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

8. (Currently Amended) The integrated circuit device of claim 1, further comprising a second conductive layer above ~~said~~ the programmable resistive material.

9. (Currently Amended) The integrated circuit device of claim 8, wherein ~~said~~ the second conductive layer comprises titanium nitride or carbon.

10. (Currently Amended) The integrated circuit device of claim 8, further comprising a conductive barrier layer between ~~said~~ the programmable resistive material and ~~said~~ the second conductive layer.

11. (Currently Amended) The integrated circuit device of claim 1, further comprising a second conductive layer in direct contact with ~~said~~ the programmable resistive material.

12. (Currently Amended) The integrated circuit device of claim 1, further comprising a second conductive layer above ~~said~~ the programmable resistive material and an interlayer dielectric over ~~said~~ the second conductive layer, ~~said~~ the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of ~~said~~ the second conductive layer.

13. (Currently Amended) The integrated circuit device of claim 12, further comprising a conductive grid interconnect within ~~said~~ the aperture.

14. (Currently Amended) The integrated circuit device of claim 13, wherein ~~said~~ the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

15. (Currently Amended) The integrated circuit device of claim 1, wherein a portion of ~~said~~ the at least one protrusion comprises a frustoconical tip.

16. (Currently Amended) The integrated circuit device of claim 15, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

17. (Currently Amended) The integrated circuit device of claim 15, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of about 0.4~~μm~~ μm.

18. (Currently Amended) The integrated circuit device of claim 15, wherein ~~said~~ the frustoconical tip has a height of approximately 2000 Å.

19. (Currently Amended) The integrated circuit device of claim 1, further comprising an opening through ~~said~~ the insulative layer such ~~said~~ that the at least part of ~~said~~ the first conductive layer is exposed.

20. (Currently Amended) The integrated circuit device of claim 19, wherein ~~said~~ the programmable resistive material is at least within ~~said~~ the opening.

21. (Currently Amended) An integrated circuit device ~~comprising,~~ comprising:

a first electrode having a first portion and a second portion, a width of the first electrode narrowing substantially and continuously in a direction extending from the second portion toward ~~said~~ the first portion of the first electrode;

a layer of programmable resistive material in contact with ~~said~~ the first portion of ~~said~~ the first

electrode; and

a second electrode coupled to the layer of programmable resistive material.

22. (Currently Amended) The integrated circuit device of claim 21, wherein ~~said~~ the programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

23. (Currently Amended) The integrated circuit device of claim 21, wherein ~~said~~ the programmable resistive material comprises a chalcogenide material.

24. (Currently Amended) The integrated circuit device of claim 23, wherein ~~said~~ the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

25. (Currently Amended) The integrated circuit device of claim 23, wherein ~~said~~ the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

26. (Original) The integrated circuit device of claim 25, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

27. (Currently Amended) The integrated circuit device of claim 21, wherein ~~said~~ the second electrode comprises titanium nitride or carbon.

28. (Currently Amended) The integrated circuit device of claim 21, further comprising a conductive barrier layer between ~~said~~ the programmable resistive material and ~~said~~ the second electrode.

29. (Currently Amended) The integrated circuit device of claim 21, wherein ~~said~~ the second electrode is in direct contact with ~~said~~ the programmable resistive material.

30. (Currently Amended) The integrated circuit device of claim 21, further comprising an interlayer dielectric over ~~said~~ the second electrode, ~~said~~ the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of ~~said~~ the second electrode.

31. (Currently Amended) The integrated circuit device of claim 30, further comprising a conductive grid interconnect within ~~said~~ the aperture.

32. (Currently Amended) The integrated circuit device of claim 31, wherein ~~said~~ the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

33. (Currently Amended) The integrated circuit device of claim 21, wherein ~~said~~ the first portion of ~~said~~ the first electrode comprises a frustoconical tip.

34. (Currently Amended) The integrated circuit device of claim 33, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

35. (Currently Amended) The integrated circuit device of claim 34, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of about 0.4~~μm~~ μm.

36. (Currently Amended) The integrated circuit device of claim 33, wherein ~~said~~ the frustoconical tip has a height of approximately 2000 Å.

37. (Currently Amended) The integrated circuit device of claim 21, further comprising an insulative layer above ~~said~~ the first electrode.

38. (Currently Amended) The integrated circuit device of claim 37, further comprising an opening through ~~said~~ the insulative layer such that at least part of ~~said~~ the first portion of ~~said~~ the first electrode is exposed.

39. (Currently Amended) The integrated circuit device of claim 38, wherein ~~said~~ the programmable resistive material is at least within ~~said~~ the opening.

40. (Currently Amended) An integrated circuit device comprising:

a first electrode having a first portion and a second portion, a width of the first electrode narrowing substantially and continuously in a direction extending from the second portion toward ~~said~~ the first portion of the first electrode;

a layer of programmable resistive material in a recess in insulative material overlying ~~said~~ the first electrode such that ~~said~~ the programmable resistive material is in contact with ~~said~~ the first electrode; and

a second electrode coupled to the layer of programmable resistive material.

41. (Currently Amended) The integrated circuit device of claim 40, wherein ~~said~~ the programmable resistive material is formulated to be reversibly cycled between at least two different resistive states.

42. (Currently Amended) The integrated circuit device of claim 40, wherein ~~said~~ the programmable resistive material comprises a chalcogenide material.

43. (Currently Amended) The integrated circuit device of claim 42, wherein ~~said~~ the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

44. (Currently Amended) The integrated circuit device of claim 43, wherein ~~said~~ the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

45. (Original) The integrated circuit device of claim 44, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

46. (Currently Amended) The integrated circuit device of claim 40, wherein ~~said~~ the second electrode comprises titanium nitride or carbon.

47. (Currently Amended) The integrated circuit device of claim 40, further comprising a conductive barrier layer between ~~said~~ the programmable resistive material and ~~said~~ the second electrode.

48. (Currently Amended) The integrated circuit device of claim 40, wherein ~~said~~ the second electrode is in direct contact with ~~said~~ the programmable resistive material.

49. (Currently Amended) The integrated circuit device of claim 40, further comprising an interlayer dielectric over ~~said~~ the second electrode, ~~said~~ the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of ~~said~~ the second electrode.

50. (Currently Amended) The integrated circuit device of claim 49, further comprising a conductive grid interconnect within ~~said~~ the aperture.

51. (Currently Amended) The integrated circuit device of claim 50, wherein ~~said~~ the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

52. (Currently Amended) The integrated circuit device of claim 40, wherein at least a part of ~~said~~ the first portion of ~~said~~ the first electrode comprises a frustoconical tip.

53. (Currently Amended) The integrated circuit device of claim 52, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

54. (Currently Amended) The integrated circuit device of claim 52, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of about 0.4~~μm~~ μm.

55. (Original) The integrated circuit device of claim 54, wherein ~~said~~ the frustoconical tip has a height of approximately 2000 Å.

56. (Currently Amended) A semiconductor memory cell comprising:

a first conductive layer on a substrate, wherein ~~said~~ the first conductive layer includes at least one raised portion;

a programmable resistive material in direct contact with ~~said~~ the at least one raised portion of ~~said~~ the first conductive layer; and

a second conductive layer above ~~said~~ the programmable resistive material.

57. (Currently Amended) The semiconductor memory cell of claim 56, wherein ~~said~~ the programmable resistive material comprises a chalcogenide material.

58. (Currently Amended) The semiconductor memory cell of claim 57, wherein ~~said~~ the chalcogenide material is selected from a group consisting of tellurium (Te), germanium (Ge), antimony (Sb), and combinations thereof.

59. (Currently Amended) The semiconductor memory cell of claim 57, wherein ~~said~~ the chalcogenide material includes tellurium (Te), germanium (Ge), and antimony (Sb) in a ratio of $Te_aGe_bSb_{100-(a+b)}$, where a, b, and 100-(a+b) are in atomic percentages which total 100% of the constituent elements and $a \leq 70$ and $15 \leq b \leq 50$.

60. (Original) The semiconductor memory cell of claim 59, wherein $40 \leq a \leq 60$ and $17 \leq b \leq 44$.

61. (Currently Amended) The semiconductor memory cell of claim 56, further comprising a conductive barrier layer between ~~said~~ the programmable resistive material and ~~said~~ the second conductive layer.

62. (Currently Amended) The semiconductor memory cell of claim 56, wherein ~~said~~ the second conductive layer is in direct contact with ~~said~~ the programmable resistive material.

63. (Currently Amended) The semiconductor memory cell of claim 56, further comprising an interlayer dielectric over ~~said~~ the second conductive layer, ~~said~~ the interlayer dielectric including an aperture that exposes at least a portion of an upper surface of ~~said~~ the second conductive layer.

64. (Currently Amended) The semiconductor memory cell of claim 63, further comprising a conductive grid interconnect within ~~said~~ the aperture.

65. (Currently Amended) The semiconductor memory cell of claim 64, wherein ~~said~~ the conductive grid interconnect is selected from the group consisting of titanium, titanium nitride and aluminum.

66. (Currently Amended) The semiconductor memory cell of claim 56, wherein a portion of ~~said~~ the at least one raised portion comprises a frustoconical tip.

67. (Currently Amended) The semiconductor memory cell of claim 66, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of at least 0.1 μm.

68. (Currently Amended) The semiconductor memory cell of claim 66, wherein ~~said~~ the frustoconical tip has a frustum lateral dimension of about 0.4~~μm~~ μm.

69. (Currently Amended) The semiconductor memory cell of claim 66, wherein ~~said~~ the frustoconical tip has a height of approximately 2000 Å.

70. (Currently Amended) The semiconductor memory cell of claim 56, wherein ~~said~~ the second conductive layer comprises titanium nitride or carbon.

71. (Currently Amended) The semiconductor memory cell of claim 56, further comprising an insulative material over ~~said~~ the first conductive layer and having an opening therethrough such that at least a portion of ~~said~~ the first conductive layer is exposed.

72. (Currently Amended) The semiconductor memory cell of claim 71, wherein ~~said~~ the programmable resistive material is at least within ~~said~~ the opening.